New Paltz
STATE UNIVERSITY OF NEW YORK
Division of Engineering Programs

EGC221: Digital Logic Lab

Experiment #2

Basic Logic Gate Physical Verification

Student's Name:	Reg. no.:
Student's Name:	Reg. no.:
Semester: Fall 2021	Date: 03 February 2021

Assessment:

Assessment Point	**Weight**	**Grade**
Methodology and correctness of results		
Discussion of results		
Participation		
Assessment Points' Grade:		

Comments:

Experiment #2:

Basic Logic Gates

Objectives:

The objectives of this experiment are to:

1. Introduce students to the tools, facilities and components needed for the experiments in digital electronics,
2. Relate voltage levels and electrical connections to digital logic levels, and
3. Verify the operation of the basic logic gates.

Discussion:

Digital electronic circuits are built using logic gates. Each logic gate implements a logic function such as the NOT (also known as the inverter), the AND, the OR and the Exclusive OR (also known as the EX-OR gate). In some cases the output of a gate is internally inverted. The AND gate with the output inverted is called the NAND gate. The OR gate with the output inverted is called the NOR gate. The EX-OR gate with the output inverted is called the EX-NOR gate.

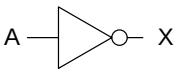
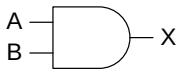
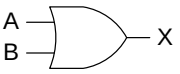
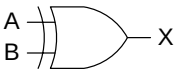
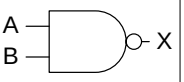
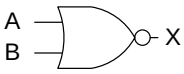
(i)	NOT	AND	OR	EX-OR	NAND	NOR
(ii)						
(iii)	$X = \overline{A}$	X = A B	X = A + B	$X = A \oplus B$	$X = \overline{A\,B}$	$X = \overline{A + B}$
(iv)	A X 0 1 1 0	A B X 0 0 0 0 1 0 1 0 0 1 1 1	A B X 0 0 0 0 1 1 1 0 1 1 1 1	A B X 0 0 0 0 1 1 1 0 1 1 1 0	A B X 0 0 1 0 1 1 1 0 1 1 1 0	A B X 0 0 1 0 1 0 1 0 0 1 1 0

Figure 1. Basic Logic Gates.

Figure 1 shows the basic logic gates. Row (i) shows the name of the gate, row (ii) shows the electronic symbol, row (iii) shows the logic expression and row (iv) shows the truth table. A truth table is a table showing all possible values at the inputs of a digital circuit and the corresponding value of the output.

Procedure:

Use a Digital I/O Module, DC Power Supply, Breadboard, Wires, and 74xx Logic ICs to solve the following exercises.

Digital I/O Module

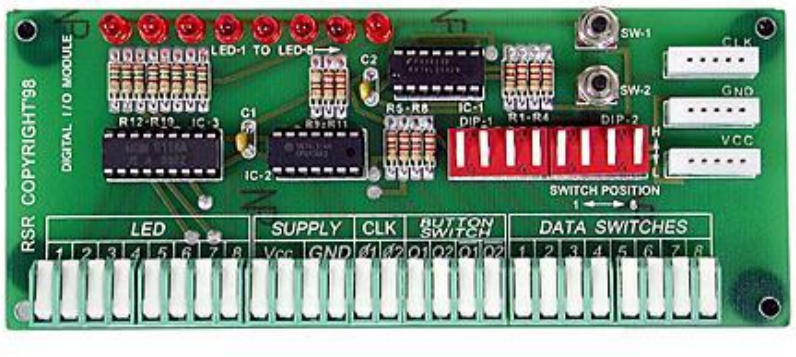


Figure 2. Digital I/O Module

DC Power Supply (see the following video: https://www.youtube.com/watch?v=b4jLZWiaoq0)

Figure 3. DC Power Supply

Breadboard (see the following URL: https://learn.sparkfun.com/tutorials/how-to-use-a-breadboard)

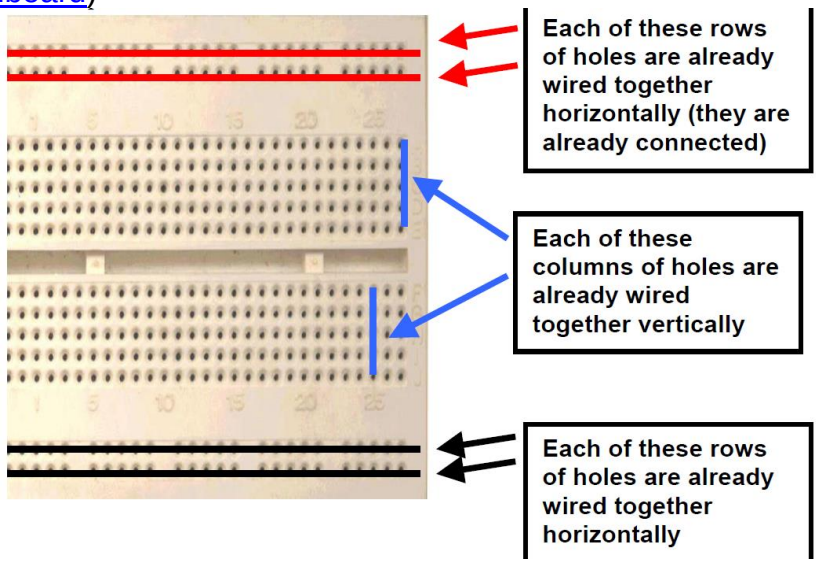


Figure 4. Breadboard

(a) Verify the operation of a single NAND gate using a Digital I/O Module, DC Power Supply, Breadboard, 7400 NAND IC, and Wires. Complete **Figure 6** and **Table 1**.

NAND Gate Integrated Circuit – the 7400 Quad 2-input NAND. See the following URL: https://www.fairchildsemi.com/datasheets/74/74F00.pdf

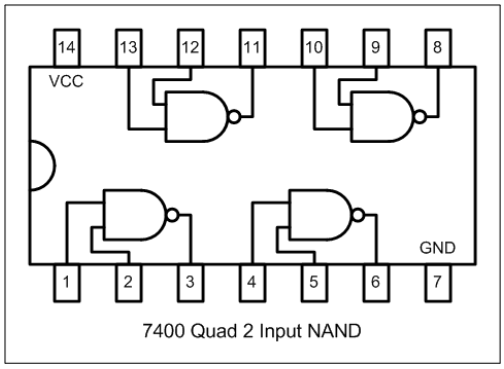


Figure 5. 7400 Quad 2-input NAND

[Insert Photo of circuit here]

Figure 6. NAND Gate Circuit.

Table 1. NAND Truth Table.

A	B	A NAND B
0	0	
0	1	
1	0	
1	1	

(b) Verify the operation of a single NOT gate using a Digital I/O Module, DC Power Supply, Breadboard, 7404 NOT IC, and Wires. Complete **Figure 8** and **Table 2**.

NOT Gate Integrated Circuit – the 7404 Hex Inverter. See the following URL: https://www.fairchildsemi.com/datasheets/74/74F04.pdf

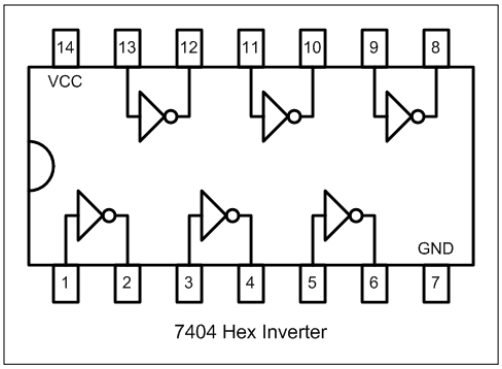


Figure 7. 7404 Hex Inverter

[Insert Photo of circuit here]

Figure 8. NOT Gate Circuit.

Table 2. NOT Truth Table.

A	NOT A
0	
1	

(c) Verify the operation of a single OR gate using a Digital I/O Module, DC Power Supply, Breadboard, 7432 OR IC, and Wires. Complete **Figure 10** and **Table 3**.

OR Gate Integrated Circuit – the 7432 Quad 2-input OR. See the following URL: https://www.fairchildsemi.com/datasheets/74/74F32.pdf

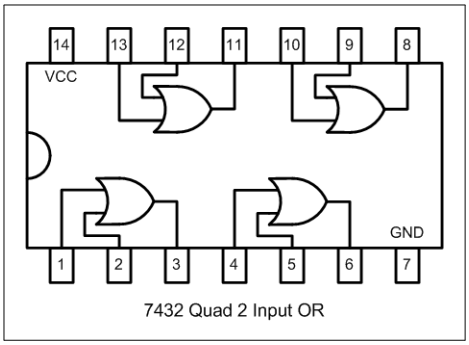


Figure 9. 7432 Quad 2-input OR

[Insert Photo of circuit here]

Figure 10. OR Gate Circuit.

Table 3. OR Truth Table.

A	B	A OR B
0	0	
0	1	
1	0	
1	1	

(d) Verify the operation of a single NOR gate using a Digital I/O Module, DC Power Supply, Breadboard, 7402 NOR IC, and Wires. Complete **Figure 12** and **Table 4**.

NOR Gate Integrated Circuit – the 7402 Quad 2-input NOR. See the following URL: https://www.fairchildsemi.com/datasheets/74/74F02.pdf

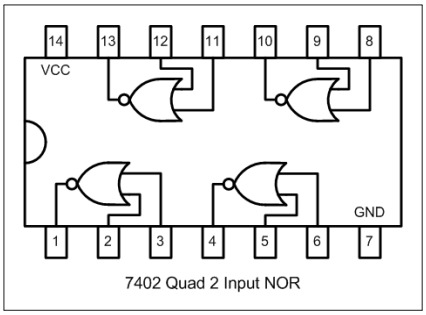


Figure 11. 7402 Quad 2-input NOR

[Insert Photo of circuit here]

Figure 12. NOR Gate Circuit.

Table 4. NOR Truth Table.

A	B	A NOR B
0	0	
0	1	
1	0	
1	1	

(e) Verify the operation of a single XOR gate using a Digital I/O Module, DC Power Supply, Breadboard, 7486 XOR IC, and Wires. Complete **Figure 14** and **Table 5**.

XOR Gate Integrated Circuit – the 7486 Quad 2-input XOR. See the following URL: https://www.fairchildsemi.com/datasheets/74/74F86.pdf

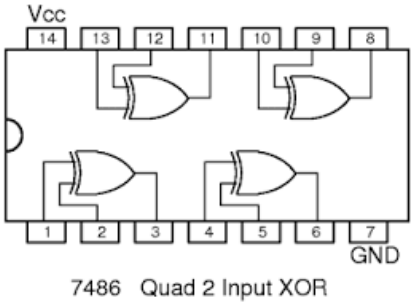


Figure 13. 7486 Quad 2-input XOR

[Insert Photo of circuit here]

Figure 14. XOR Gate Circuit.

Table 5. XOR Truth Table.

A	B	A XOR B
0	0	
0	1	
1	0	
1	1	

(f) Verify the operation of a single AND gate using a Digital I/O Module, DC Power Supply, Breadboard, 7400 NAND IC, and Wires. Complete **Figures 17 and 18** and **Tables 6 and 7**.

Hint: Since we do not have 7408 Quad 2-input ANDs in stock, you will need to use combinational logic circuit theory design, and a 7400 NAND IC to create the AND circuit.

AND Gate Integrated Circuit – the 7408 Quad 2-input NAND. See the following URL: https://www.fairchildsemi.com/datasheets/74/74F08.pdf

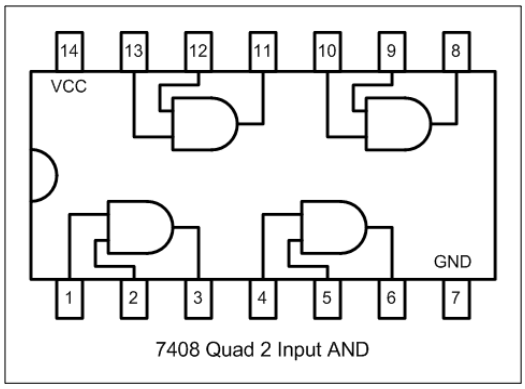


Figure 15. 7408 Quad 2-input AND

NAND Gate Integrated Circuit – the 7400 Quad 2-input NAND. See the following URL: https://www.fairchildsemi.com/datasheets/74/74F00.pdf

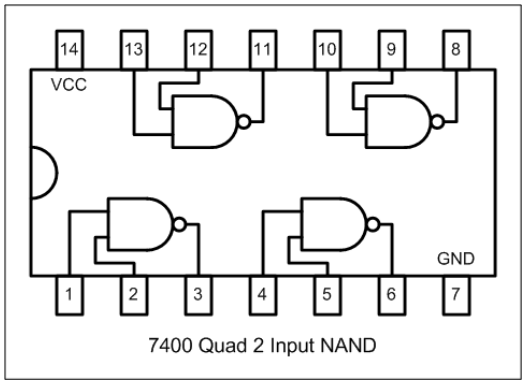


Figure 16. 7400 Quad 2-input NAND

First use LOGISIM to design and simulate your AND circuit (using NAND gates only.) Complete **Figure 17** and **Table 6**.

[Insert Photo of circuit here]

Figure 17. AND Gate Circuit.

Table 6. Simulated AND Truth Table.

A	B	A AND B
0	0	
0	1	
1	0	
1	1	

Next build your AND circuit and verify its operation (using NAND gates only.) Complete **Figure 18** and **Table 7**.

[Insert Photo of circuit here]

Figure 18. AND Gate Circuit.

Table 7. Implemented AND Truth Table.

A	B	A AND B
0	0	
0	1	
1	0	
1	1	

Conclusions (discussion of results):